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10/008,704	12/06/2001	Sang-Ho Ahn	9903-045	8392

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EXAMINER	
TRAN, TAN N	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 12/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/008,704	Applicant(s) AHN ET AL.	
	Examiner TAN N TRAN	Art Unit 2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *amendment filed on 10/15/03* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *20-141* is/are pending in the application.

4a) Of the above claim(s) *30-49* is/are withdrawn from consideration.

5)☒ Claim(s) *137-141* is/are allowed.

6)☒ Claim(s) *20-29 and 50-136* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. In response to the request to continue examination, note that "The examiner made a mistake when using control serial number of this application to send advisory action to applicant, but the advisory action should be the other application", therefore, last advisory action are accordingly withdrawn. However, a new rejection is set forth further below. This action is not made final.

2. The indicated allowability of claim 20-29,50-54,58,65,74,81, 87-115 withdrawn in view of the old discovered reference(s) to claim 20-29,50-54,58,65,74,81, 87-115. Rejections based on the old cited reference(s) follow.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 55-57,59,62-64 are rejected under 35 U.S.C. 102(b) as being anticipated by Casto et al. (5,014,113).

With regard to claim 55, Casto et al. discloses a lead frame comprising a die pad 40, a plurality of leads 28 disposed around the die pad 40 and a tie bars 46 connected to and disposed around the die pad 40, wherein the die pad 40 comprises a chip attaching part and a peripheral

part surrounding the chip attaching part; a semiconductor chip 12 mounted to the die pad chip attaching part, the chip 12 having a plurality of electrode pads 14, wherein the plurality of electrode pads 14 are electrically interconnected to the leads 28, and wherein each of leads 28 comprises integrally connected inner leads and outer leads; an encapsulant encapsulating the semiconductor chip 12 to form a package body 36, wherein the inner leads are encapsulated by the encapsulant and the outer leads are external to the encapsulant; and the chip attaching part having a first thickness and the inner leads 28 totally having a constant second thickness greater than the first thickness wherein the chip attaching part and the peripheral part have the same thickness. (Note figs.1, 2 of Casto et al.).

With regard to claim 56, Casto et al. discloses the inner leads are formed of a single layer. (Note figs.1, 2 of Casto et al.).

With regard to claim 57, Casto et al. discloses the first thickness is between about 30 percent to 50 percent of the second thickness. (Note lines 20-24, column 5, figs.1,2 of Casto et al.).

With regard to claim 59, Casto et al. discloses the die pad 40 is located below the leads 28. (Note fig.1 of Casto et al.).

With regard to claim 62, Casto et al. discloses upper and lower portions of the package body with reference to the leads (18,28) have different thickness each other. (Note fig.1 of Casto et al.).

With regard to claim 63, Casto et al. discloses the tie bar 46 has the same thickness as the leads 18. (Note figs.1,2 of Casto et al.).

With regard to claim 64, Casto et al. discloses the tie bar 46 has the same thickness as the die pad peripheral part. (Note figs.1,2 of Casto et al.).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 20-24,28,50-54,58,71-81,86-96,100,102-110,114,116-127,132-134,136 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nokita (JP-2000-124396) in view of Casto et al. (5,014,113).

With regard to claims 20,21,22,50,52,54,58,71,74,75,87,88,102,116,120,121,133,134, Nokita discloses a semiconductor package device having 0.5mm or less of thickness comprising: a lead frame comprising a die pad 1, a plurality of leads 2 disposed around the die pad 1 wherein the die pad 1 comprises a chip attaching part having a first thickness and disposed below the leads 2; a peripheral part surrounding and protruding away the chip attaching part; first and second semiconductor chips 5 mounted to the die pad chip attaching part, wherein the first semiconductor chip is bonded to a top surface of the chip attaching part and the second semiconductor chip is bonded to a bottom surface of the chip attaching part; a package body 8 encapsulating the semiconductor chips 5; and bonding wires 7 configured to electrically connect the semiconductor chips 5 and leads 2, leads 2 having the inner leads are encapsulated by the

package body 8 and the outer leads are exposed from the package body 8; wherein the inner leads having a second thickness, wherein the first thickness is smaller than the second thickness, wherein the peripheral part have a thickness equal to the second thickness of the inner leads, and wherein the peripheral part protrudes toward the second semiconductor chip, wherein the bonding wires 7A connected to one of the semiconductor chips 5 are shorter than the bonding wires 7B connected to the other semiconductor chip. (Note lines 1,2, paragraph 0014, fig.1 of Nokita).

Nokita does not disclose the first and second semiconductor chips each having a plurality of electrode pads and a tie bar connected to the die pad.

However, Casto et al. discloses the chip 12 having a plurality of electrode pads 14, wherein the plurality of electrode pads 14 are electrically interconnected to the leads 28, a tie bars 46 connected to and disposed around the die pad 40. (Note figs.1, 2 of Casto et al.).

Therefore, it would have been obvious to one of ordinary skill in the art to form the Nokita's device having the first and second semiconductor chips each having a plurality of electrode pads and a tie bar connected to the die pad such as taught by Casto et al. in order to secure an electrical connection between the semiconductor chips 5 and leads 2, and secure the interface between semiconductor chips and the die pads.

With regard to claims 23,76,91,105,122, Nokita and Casto et al. do not disclose bonding wires are connected by balls formed on the surface of the leads and stiches formed on the electrode pads. However, it would have been obvious to one of ordinary skill in the art to form bonding wires are connected by balls formed on the surface of the leads and stiches formed on

the electrode pads in order to secure the electrical connection between semiconductor chips and the leads.

With regard to claims 24,77,92,106,123, Nokita and Casto et al. do not disclose metal bumps are formed on the electrode pads of the chip and wherein the stiches are formed on the metal bumps. However, it would have been obvious to one of ordinary skill in the art to form metal bumps are formed on the electrode pads of the chip and wherein the stiches are formed on the metal bumps in order to secure the interface between semiconductor chips and the die pads.

With regard to claim 28, Nokita and Casto et al. disclose all the claimed subject matter except for a thickness of the package body is about 580 micrometer, a thickness of the die pad peripheral part is about 100 micrometer, and a thickness of the chip attaching part is about 40 micrometer. However, it would have been obvious to one of ordinary skill in the art to form for a thickness of the package body is about 580 micrometer, a thickness of the die pad peripheral part is about 100 micrometer, and a thickness of the chip attaching part is about 40 micrometer in order to simplify the structure and fabrication to reduce the assembly cost of the device and to reduce the thickness or height of the device, because such structure is conventional in the art for forming a compact multi-chip package.

With regard to claims 51,53,86,100,114,132, Nokita and Casto et al. disclose all the claimed subject matter except for the electronic apparatus is a memory card. However, it would have been obvious to one of ordinary skill in the art to form the electronic apparatus is a memory card, because such structure is conventional in the art for forming a compact multi-chip package.

With regard to claims 72,89,103, Nokita discloses the inner leads of the leads 2 are formed of a single layer. (Note fig.1 of Nokita).

With regard to claims 73,90,104,118, Nokita discloses the first thickness is between about 30% to 50% of the second thickness. (Note fig.1 of Nokita).

With regard to claims 79,80,94,95,108,109, Nokita and Casto et al. do not disclose the tie bar has the same thickness as the leads wherein the tie bar has the same thickness as the die pad peripheral part. However, it would have been obvious to one of ordinary skill in the art to form disclose the tie bar has the same thickness as the leads wherein the tie bar has the same thickness as the die pad peripheral part in order to secure the interface between semiconductor chips and the die pads.

With regard to claims 81,96,110,117,127, Nokita discloses the peripheral part of the die pad 1 protrudes in both vertical directions from the chip attaching part, and the thickness of the peripheral part is equal to the thickness of the leads 2. (Note fig.1 of Nokita).

With regard to claims 78,93,107,124, Nokita and Casto et al. do not disclose an upper portion of the package body above the leads and a lower portion of the package body below the leads have different thicknesses. However, it would have been obvious to one of ordinary skill in the art to form an upper portion of the package body above the leads and a lower portion of the package body below the leads have different thicknesses because such structure is conventional in the art for forming a compact multi-chip package.

With regard to claim 136, Nokita discloses the peripheral part protrudes upward from the chip attaching part. (Note fig.1 of Nokita).

With regard to claim 119, Casto et al. discloses the chip attaching part and the peripheral part of die pad 40 have the same thickness (Note figs.1,2 of Casto et al.).

Claim 135 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nokita (JP-2000-124396) in view of Casto et al. (5,014,113) and further in view of Kouda (5,818,105).

With regard to claims 135, Nokita and Casto et al. do not disclose the peripheral part protrudes from only one side of the chip attaching part.

However, Kouda discloses the peripheral part protrudes from only one side of the chip attaching part. (Note fig. 8 of Kouda).

Therefore, it would have been obvious to one of ordinary skill in the art to form the Nokita and Casto et al.'s device having the peripheral part protrudes from only one side of the chip attaching part such as taught by Kouda in order to secure the semiconductor chip on the die pad of the lead frame.

Claims 25-27,29,82-84,97-99,111-113,128-130 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nokita (JP-2000-124396) in view of Casto et al. (5,014,113) and further in view of Huang (2002/0113305).

With regard to claims 25,82,83,97,98,111,112,128,129, Nokita and Casto et al. do not disclose the die pad comprises divided first and second die pads wherein the first and second die pads each include a chip attaching part and peripheral part.

However, Huang discloses the die pad comprises divided first and second die pads (410,440) wherein the first and second die pads (410,440) each include a chip attaching part and peripheral part. (Note fig. 1 of Huang).

Therefore, it would have been obvious to one of ordinary skill in the art to form the Nokita and Casto et al.'s device having the die pad comprises divided first and second die pads

wherein the first and second die pads each include a chip attaching part and peripheral part such as taught by Huang in order to provide more space for accommodating semiconductor chips.

With regard to claim 26, Huang discloses the first and second die pads (410,440) each include a chip attaching part and a peripheral part. (Note fig. 1 of Huang).

With regard to claims 27,29,84,99,113,130, Nokita and Casto et al. do not disclose an adhesive bonds the semiconductor chip to the die pad chip attaching part, and an adhesive is attached to the backside of the chip in a wafer state to bond the semiconductor chips to the chip attaching part.

However, Huang discloses an adhesive 11a bonds the semiconductor chip to the die pad chip attaching part. An adhesive 11b is attached to the backside of the chip in a wafer state to bond the semiconductor chips (12a,12b) to the chip attaching part. (Note fig. 6 of Huang).

Therefore, it would have been obvious to one of ordinary skill in the art to form the Nokita and Casto et al.'s device having an adhesive bonds the semiconductor chip to the die pad chip attaching part, and an adhesive is attached to the backside of the chip in a wafer state to bond the semiconductor chips to the chip attaching part such as taught by Huang in order to secure the interface between semiconductor chips and the die pads.

Claims 60,70 are rejected under 35 U.S.C. 103(a) as being unpatentable over Casto et al. (5,014,113).

With regard to claim 60, Casto et al. discloses the plurality of electrode pads 14 are electrically interconnected to the leads 28 via bonding wires 34.

Casto et al. does not disclose bonding wires are connected by balls formed on the surface of the leads and stiches formed on the electrode pads. However, it would have been obvious to one of ordinary skill in the art to form bonding wires are connected by balls formed on the surface of the leads and stiches formed on the electrode pads in order to secure the interface between semiconductor chips and the die pads.

With regard to claim 61, Casto et al. discloses metal bumps are formed on the electrode pads 14 of the chip 12. (Note lines 1-7, column 4, fig. 1 of Casto et al.).

Casto et al. does not disclose the stiches are formed on the metal bumps. However, it would have been obvious to one of ordinary skill in the art to form the stiches are formed on the metal bumps in order to secure the interface between semiconductor chips and the die pads. (Note lines 1-7, column 4, fig. 1 of Casto et al.).

With regard to claim 70, Casto et al. does not disclose the semiconductor chip is a memory device and wherein the adhesive is a film made of an epoxy resin. However, it would have been obvious to one of ordinary skill in the art to form the semiconductor chip is a memory device and wherein the adhesive is a film made of an epoxy resin in order to secure the semiconductor chip on the die pad of the lead frame and because such structure is conventional in the art for forming a compact multi-chip package.

Claims 65 is rejected under 35 U.S.C. 103(a) as being unpatentable over Casto et al. (5,014,113) in view of Nokita (JP-2000-124396).

With regard to claim 65, Casto et al. does not disclose the peripheral part protrudes in both vertical directions from the chip attaching part, and the thickness of the peripheral part is equal to the thickness of the leads.

However, Nokita discloses the peripheral part of the die pad 1 protrudes in both vertical directions from the chip attaching part, and the thickness of the peripheral part is equal to the thickness of the leads 2. (Note fig.1 of Nokita).

Therefore, it would have been obvious to one of ordinary skill in the art to form the Casto et al.'s device having the peripheral part protrudes in both vertical directions from the chip attaching part, and the thickness of the peripheral part is equal to the thickness of the leads such as taught by Nokita because such structure is conventional in the art for forming a compact multi-chip package.

Claims 66-68,133 are rejected under 35 U.S.C. 103(a) as being unpatentable over Casto et al. (5,014,113) in view of Huang (2002/0113305).

With regard to claim 66, Casto et al. does not disclose the die pad comprises divided first and second die pads.

However, Huang discloses the die pad comprises divided first and second die pads (410,440). (Note fig. 1 of Huang).

Therefore, it would have been obvious to one of ordinary skill in the art to form the Casto et al.'s device having the die pad comprises divided first and second die pads such as taught by Huang in order to secure semiconductor dies to be separated from the die pads of the leadframe.

With regard to claim 67, Huang discloses the first and second die pads (410,440) each include a chip attaching part and a peripheral part. (Note fig. 1 of Huang).

With regard to claim 68, Casto et al. does not disclose an adhesive bonds the semiconductor chip to the die pad chip attaching part.

However, Huang discloses an adhesive 11a bonds the semiconductor chip to the die pad chip attaching part. (Note fig. 6 of Huang).

Therefore, it would have been obvious to one of ordinary skill in the art to form the Casto et al.'s device having an adhesive bonds the semiconductor chip to the die pad chip attaching part such as taught by Huang in order to secure the interface between semiconductor chips and the die pads.

With regard to claim 133, Huang discloses the semiconductor chip 12a and another semiconductor chip 12b are of the same type. (Note fig. 6 of Huang).

Claims 69,85,101,115,131 rejected under 35 U.S.C. 103(a) as being unpatentable over Casto et al. (5,014,113) in view of Kozono (6,177,718).

With regard to claims 69,85,101,115,131, Casto et al. does not disclose the lead frame is made of iron-nickel alloy or copper alloy, and wherein the bonding wires are gold wires.

However, Kozono discloses the lead frame 13 is made of iron-nickel alloy or copper alloy, and wherein the bonding wires 14 are gold wires. (Note lines 16-20, column 6, fig. 21 of Kozono).

Therefore, it would have been obvious to one of ordinary skill in the art to form the Casto et al.'s device having the lead frame is made of iron-nickel alloy or copper alloy, and wherein the bonding wires are gold wires such as taught by Kozono in order to prevent the lead frame from broken.

Allowable Subject Matter

4. Claims 137-141 allowable over the prior art of record, because none of these references disclose or can be combined to yield the claimed invention such as the peripheral part only protrudes downward as recited in claim 137.

Response to Amendment

5. Applicant's arguments with respect to claims 20-29,50-136 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Tan Tran whose telephone number is (703) 305-3362. The examiner can normally be reached on M-F 8:30AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for after final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

TT

Nov 2003

Minhloan Tran
Primary Examiner
Art Unit 2826